REMARKS

Claims 1 through 6 and 8 through 24 are currently pending in the above-referenced application. Each of claims 1 through 6 and 8 through 24 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(b)

Claims 1 through 6 and 8 through 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,786,628 to Beilstein, Jr. et al. (hereinafter "Beilstein").

Applicant submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Beilstein describes electronic modules 11 that include multiple integrated circuit chips 13 stacked in back side-to-active surface arrangement. So-called "transfer metal 15", or wiring, is positioned across the active surface of each chip 13 of the module 11 to establish communication between an I/O pad (not shown), or bond pad, on the active surface of the chip 13 and a corresponding electrical contact, referred to in Beilstein as "BLM pads 27," formed on a common side surface 25 of an insulation layer 21 of the module 11, the side surface 25 of the insulation layer being located opposite from the chips 13 of the module 11. Col. 8, lines 4-7, 33-36. A bump 29 of conductive material is secured to each BLM pad 27. Col. 8, lines 54-57.

The transfer metal 15 described in Beilstein is not a bond pad. The term "bond pad" is defined by ICKnowledge, available at www.icknowledge.com, which provides definitions for several terms that are commonly used in the semiconductor device industry, as a "metal pad[] on [a] semiconductor die where wire bonds can be attached to connect the die to the outside world." The text Van Zant, P., Microchip Fabrication, page 502 (2d ed., McGraw-Hill, 1990), also defines bond pads as the "relatively rectangular or square areas of metallization on a die that are the sites for electrical testing (probing) and are utilized to electrically attach the chip lead system to its package." Accordingly, it is clear that the I/O pad to which the transfer metal 15 of Beilstein

is secured, not the transfer metal 15 itself, is a bond pad. Instead, the transfer metal 15 described in Beilstein acts as a wire or lead that facilitates communication between the integrated circuitry of a chip 13 associated with a particular bond pad, or "I/O pad," and circuitry which is external to the chip 13.

It has also been asserted, at page 6 of the Office Action dated September 23, 2002, that Beilstein inherently describes bond pads which are substantially in-line. First, the transfer metal 15 described in Beilstein is not a "bond pad," as that term is generally defined in the relevant art. Rather, the only bond pads that are described in Beilstein are the I/O pads of the chips 13, to which the transfer metals 15 are secured. Second, the standard is high when a rejection under 35 U.S.C. § 102 includes an assertion that one or more claim elements are inherently described by a reference:

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert,* 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) . . .; *In re Oelrich,* 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). 'To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized be persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient,'' *In re Robertson,* 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

M.P.E.P. § 2112.

As transfer metal 15 is used in the module 11 of Beilstein to provide an electrical link between the I/O pads of each chip 13 of the module 11 and circuitry which is external to that chip 13, it is clear that the I/O pads of each chip 13 need not be in-line with one another.

Moreover, because Beilstein teaches that transfer metal 15 is needed to provide an electrical connection between the I/O pads of each chip 13 and their corresponding BLM pads 27 of the module 11, Beilstein clearly lacks any express or inherent description that the I/O pads are positioned adjacent an edge of the chip 13.

As FIG. 7 of Beilstein clearly illustrates each BLM pad 27 of the described module 11 as being located on an opposite side of the insulation layer 21 from that against which the chips 13 and transfer metal 15 are positioned, it is evident that the bumps 29 that are secured to the BLM pads 27 are remote from, not adjacent to, the corresponding I/O pads of the chip 13.

In view of the foregoing, it is apparent that Beilstein lacks any express or inherent description of several of the elements of independent claim 1, as amended and presented herein. In particular, Beilstein lacks any express or inherent description of a semiconductor device (*e.g.*, chip 13) which includes a plurality of bond pads (*e.g.*, I/O pads) disposed adjacent and edge of a surface thereof. Also, Beilstein neither expressly nor inherently describes a semiconductor device (*e.g.*, chip 13) which includes bond pads (*e.g.*, I/O pads) that are arranged substantially in-line with one another. Beilstein additionally lacks any express or inherent description of a semiconductor device (*e.g.*, chip 13) which includes conductive bumps (*e.g.*, bumps 29) secured to the bond pads (*e.g.*, I/O pads) thereof.

For these reasons, Beilstein cannot anticipate each and every element of independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(b).

Claims 2 through 6 and 8 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 2 is additionally allowable since Beilstein does not expressly or inherently describe that a conductive bump (*e.g.*, bump 29) may be disposed adjacent a single bond pad (*e.g.*, I/O pad) of a semiconductor device (*e.g.*, chip 13), let alone that a conductive bump may be disposed adjacent to each bond pad of a semiconductor device.

Independent claim 9, as amended and presented herein, is also allowable over Beilstein under 35 U.S.C. § 102(b) for several reasons. First, Beilstein neither expressly nor inherently describes a semiconductor device (*e.g.*, chip 13) with a plurality of bond pads (*e.g.*, I/O pads) adjacent to and edge thereof. Second, Beilstein lacks any express or inherent description that the bond pads (*e.g.*, the I/O pads) of the chip 13 described therein are arranged substantially in-line. Third, Beilstein includes no express or inherent description that conductive bumps (*e.g.*, bumps 29) may be secured to bond pads (*e.g.*, I/O pads) of a semiconductor device (*e.g.*, chip 13).

Claims 10 through 12 are each allowable, among other reasons, as depending either directly or indirectly from claim 9, which is allowable.

Claim 12 is additionally allowable since Beilstein does not expressly or inherently describe that a conductive bump (*e.g.*, bump 29) may be disposed adjacent a single bond pad (*e.g.*, I/O pad)

of a semiconductor device (*e.g.*, chip 13), let alone that a conductive bump may be disposed adjacent to each bond pad of a semiconductor device.

Independent claim 13, as amended and presented herein, is also allowable since Beilstein lacks any express or inherent description of a semiconductor device (*e.g.*, chip 13) which includes a plurality of bond pads (*e.g.*, I/O pads) adjacent to and edge thereof or a plurality of bond pads (*e.g.*, I/O pads) that are arranged substantially in-line. Also, Beilstein does not expressly or inherently describe conductive joints (*e.g.*, bumps 29) that are secured to the bond pads (*e.g.*, I/O pads) of a semiconductor device (*e.g.*, chip 13).

Each of claims 14 through 18 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 14 is also allowable since Beilstein does not expressly or inherently describe that a conductive bump (*e.g.*, bump 29) may be disposed adjacent a single bond pad (*e.g.*, I/O pad) of a semiconductor device (*e.g.*, chip 13), let alone that a conductive bump may be disposed adjacent to each bond pad of a semiconductor device.

Like independent claims 1, 9, and 13, independent claim 19, as amended and presented herein, is allowable because Beilstein does not expressly or inherently describe a semiconductor device (*e.g.*, chip 13) which includes a plurality of bond pads (*e.g.*, I/O pads) adjacent to and edge thereof or a plurality of bond pads (*e.g.*, I/O pads) that are arranged substantially in-line. In addition, Beilstein neither expressly nor inherently describes conductive joints (*e.g.*, bumps 29) that are secured to the bond pads (*e.g.*, I/O pads) of a semiconductor device (*e.g.*, chip 13).

Claims 20 through 24 are each allowable, among other reasons, as depending either directly or indirectly from claim 19, which is allowable.

Claim 20 is additionally allowable since Beilstein does not expressly or inherently describe that a conductive bump (*e.g.*, bump 29) may be disposed adjacent a single bond pad (*e.g.*, I/O pad) of a semiconductor device (*e.g.*, chip 13), let alone that a conductive bump may be disposed adjacent to each bond pad of a semiconductor device.

For these reasons, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 1 through 6 and 8 through 24 as being anticipated by Beilstein be withdrawn.

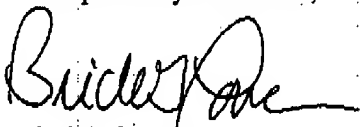
Obviousness-Type Double Patenting

Claims 1 through 24 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 21 of U.S. Patent 6,140,696. A terminal disclaimer and the appropriate fee are being filed herewith, pursuant to 37 C.F.R. § 1.321(b) and (c) to obviate the obviousness-type double patenting rejection, thereby avoiding further prosecution delay and expense. The filing of a terminal disclaimer in the above-referenced application should not be construed as acquiescence of the obviousness-type double patenting rejection.

CONCLUSION

It is respectfully submitted that each of claims 1 through 6 and 8 through 24 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: December 19, 2002

BGP/jml
Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

A marked-up version of the amended paragraph in the specification, highlighting the changes thereto, follows to clearly identify the amendments:

Please replace the first full paragraph on page 2 with the following:

Cross Reference to Related Application: This application is a continuation of application Serial No. 09/014,053, filed January 27, 1998, [pending] now U.S. Patent 6,140,696, issued October 31, 2000.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Twice amended) A vertical surface mount semiconductor device, comprising:

a semiconductor device having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line and having a plurality of conductive bumps [disposed adjacent] secured to selected bond pads, each of said conductive bumps configured to form a conductive joint between at least one of said selected bond pads and a corresponding terminal of a substrate upon positioning said semiconductor device substantially vertically relative to said substrate.

9. (Twice amended) A vertical surface mount semiconductor device, comprising:

a semiconductor device having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line, selected bond pads of said plurality of bond pads having conductive bumps [adjacent] secured thereto, said conductive bumps configured to form a joint between said selected bond pads and corresponding terminals of a carrier substrate upon substantially perpendicular orientation of said semiconductor device on said carrier substrate; and

a support member, at least a portion of which is disposed proximate said edge of said semiconductor device.

13. (Twice amended) A chip-on-board assembly, comprising:

a substrate with a plurality of terminals;

a semiconductor device configured to be positioned substantially perpendicularly relative to said substrate, said semiconductor device having a plurality of bond pads on a surface thereof, each of said plurality of bond pads being located adjacent an edge of said surface and arranged substantially in-line; and

electrically conductive joints configured to be secured to selected bond pads and to be disposed directly between and [to] establish communication between selected bond pads and corresponding terminals.

19. (Twice amended) A computer including a vertically mountable semiconductor device, the semiconductor device comprising:

a semiconductor die with a plurality of circuit traces and a plurality of bond pads disposed on a surface of said semiconductor die proximate an edge thereof in a substantially in-line arrangement, each of said plurality of bond pads communicating with one of said plurality of circuit traces; and

conductive bumps [in communication with] secured to selected bond pads, said conductive bumps each configured to form a joint between one of said selected bond pads and a corresponding terminal of a substrate when said semiconductor device is positioned substantially perpendicularly relative to said substrate.